LA-UR-03-5062

Approved for public release;
distribution is unlimited.

Title: Accelerator Validation of an FPGA SEU Simulator

Author(s):

D. Eric Johnson, LANL, BYU
Michael Caffrey, LANL
Paul Graham, LANL
Nathan Rollins, BYU
Michael Wirthlin, BYU

Submitted to:

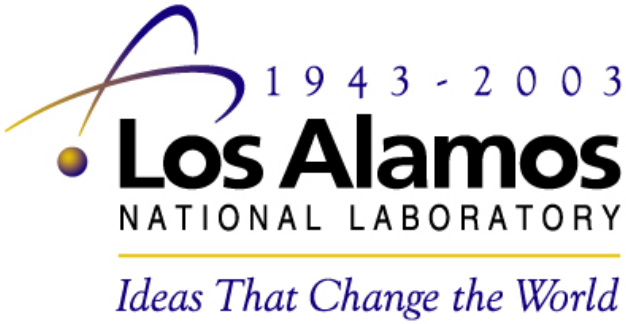
IEEE Nuclear Science Radiation Effects Conference/
IEEE Transactions on Nuclear Science
Monterey CA, USA
July 21 - 25, 2003

Accelerator Validation of an FPGA SEU Simulator

Eric Johnson[1,2], Michael Caffrey[1], Paul Graham[1], Nathan Rollins[2], Michael Wirthlin[2]

[1] Los Alamos National Laboratory

[2]Department of Electrical and Computer Engineering
Brigham Young University



This work was supported by Los Alamos National Laboratory, U.S. Department of Energy, Deployable Adaptive Systems Project (DAPS)/Cibola Flight Experiment (CFE)

Abstract: Prove Accuracy of SRAM FPGA SEU Simulator

- Prove the accuracy of results obtained with SRAM FPGA SEU simulator in ***DYNAMIC*** tests
  - Use simulator to measure sensitivity of configuration bits (those that may cause output errors) and forecast fluence per output error
  - Use accelerator to measure sensitive configuration bits and fluence per output error
  - Compare predicted to measured values
- 98% ACCURATE!

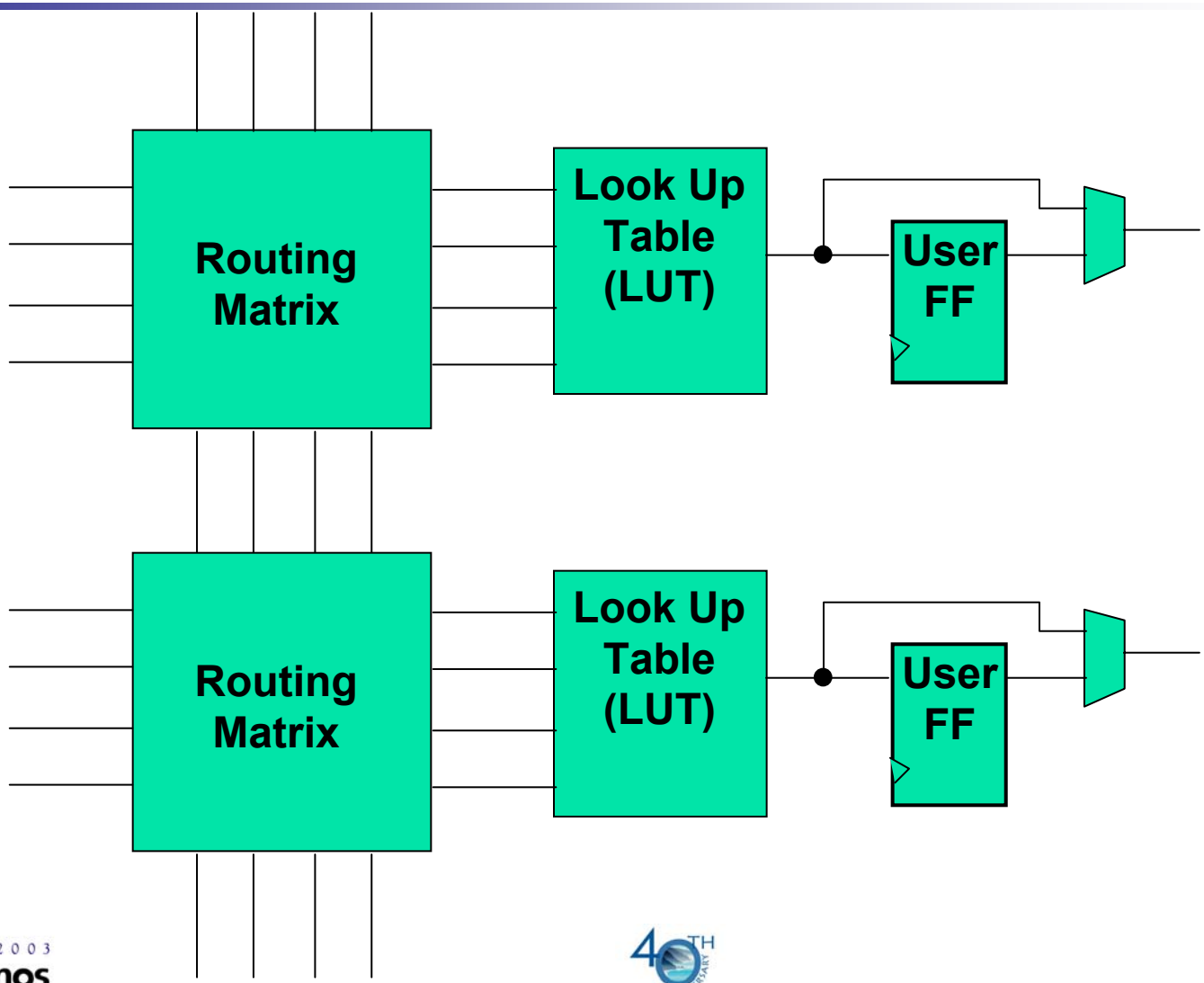
Why Use SRAM FPGAs in Space?

- *Performance*: 100x vs. radiation hardened μP (for fixed volume, power, weight), continuous processing at 100+ MS/s
- *On-orbit processing*: can improve system sensitivity and reduce communication bandwidth
- *On-orbit reprogrammability*: counteract mission obsolescence and on-orbit faults
- *Cost*: cheaper than low-volume ASICs
- *Lead time*: no ASIC design, fab, and test
- Challenge: SEUs!

Test Facility

- Crocker Nuclear Laboratory, UC Davis
- Protons 63 MeV
- Previous experiments show saturation well below 30 MeV[2]
- Protons desired: lower interaction rate than heavy ions allows slower SEU introduction rate
- Slower SEU rate necessary for dynamic testing
- Flux Range: $1 - 3.5 \times 10^7$ $P^+/cm^2/s$

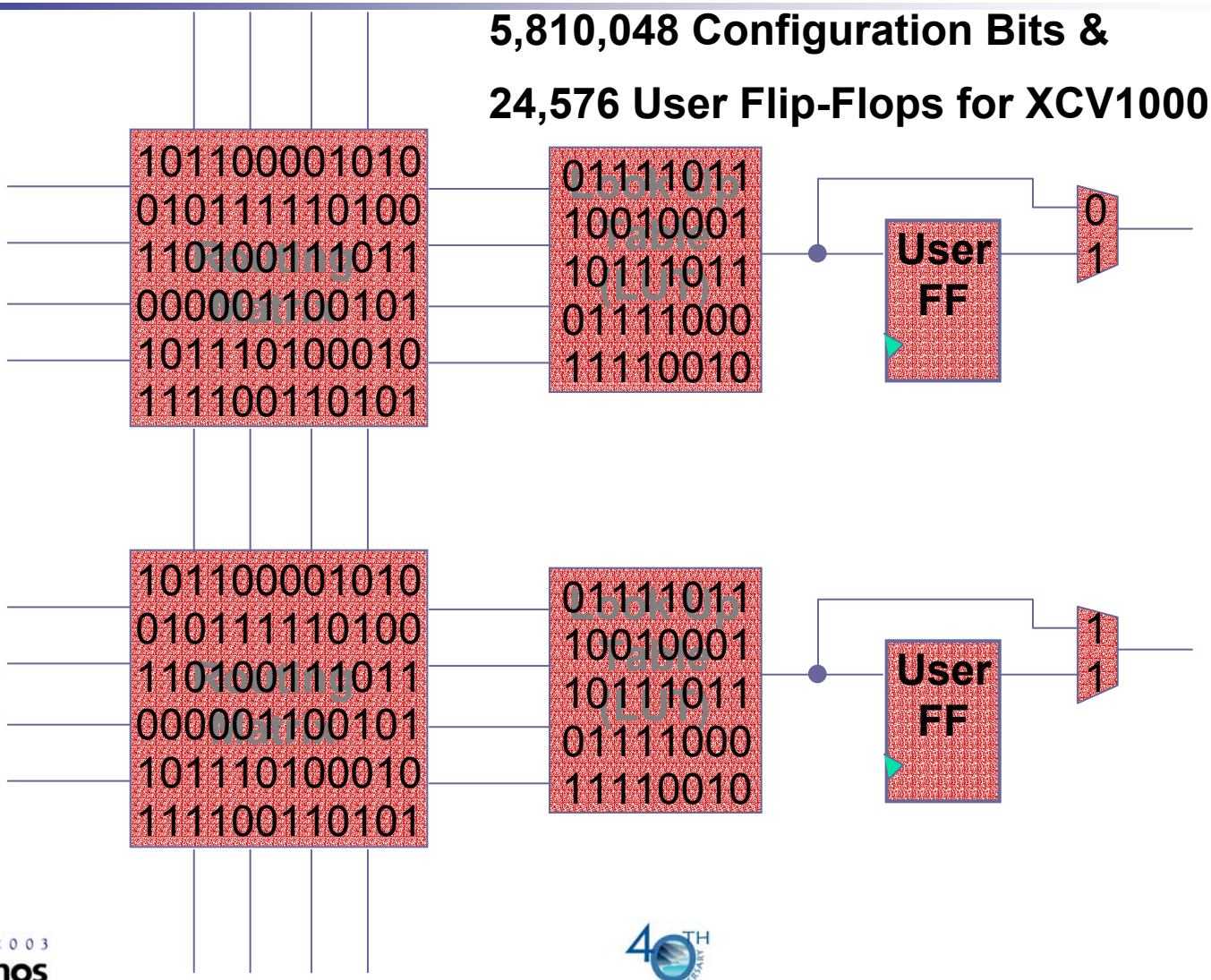
SRAM FPGA Architecture



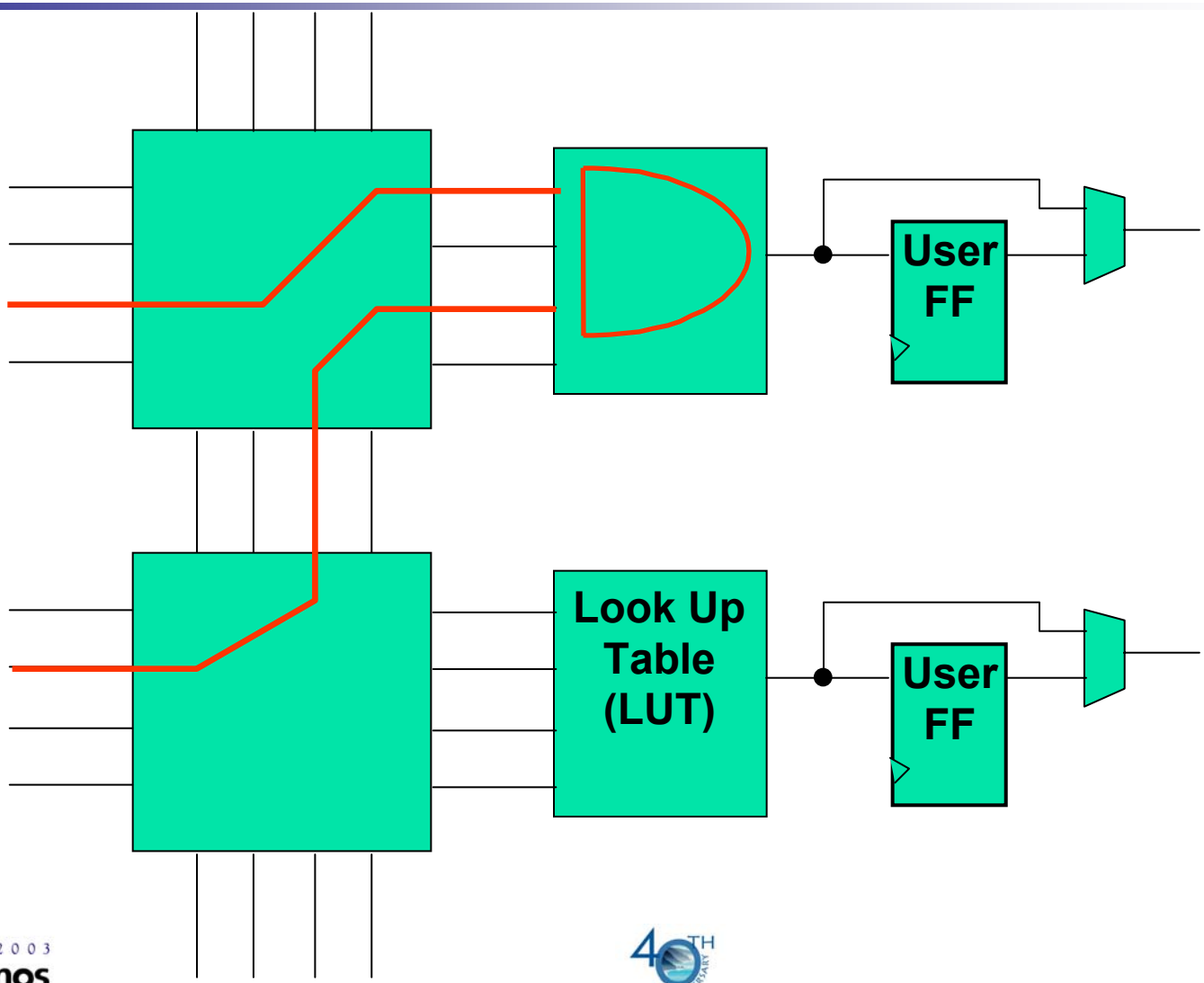
SRAM FPGA Configuration Bits

5,810,048 Configuration Bits &

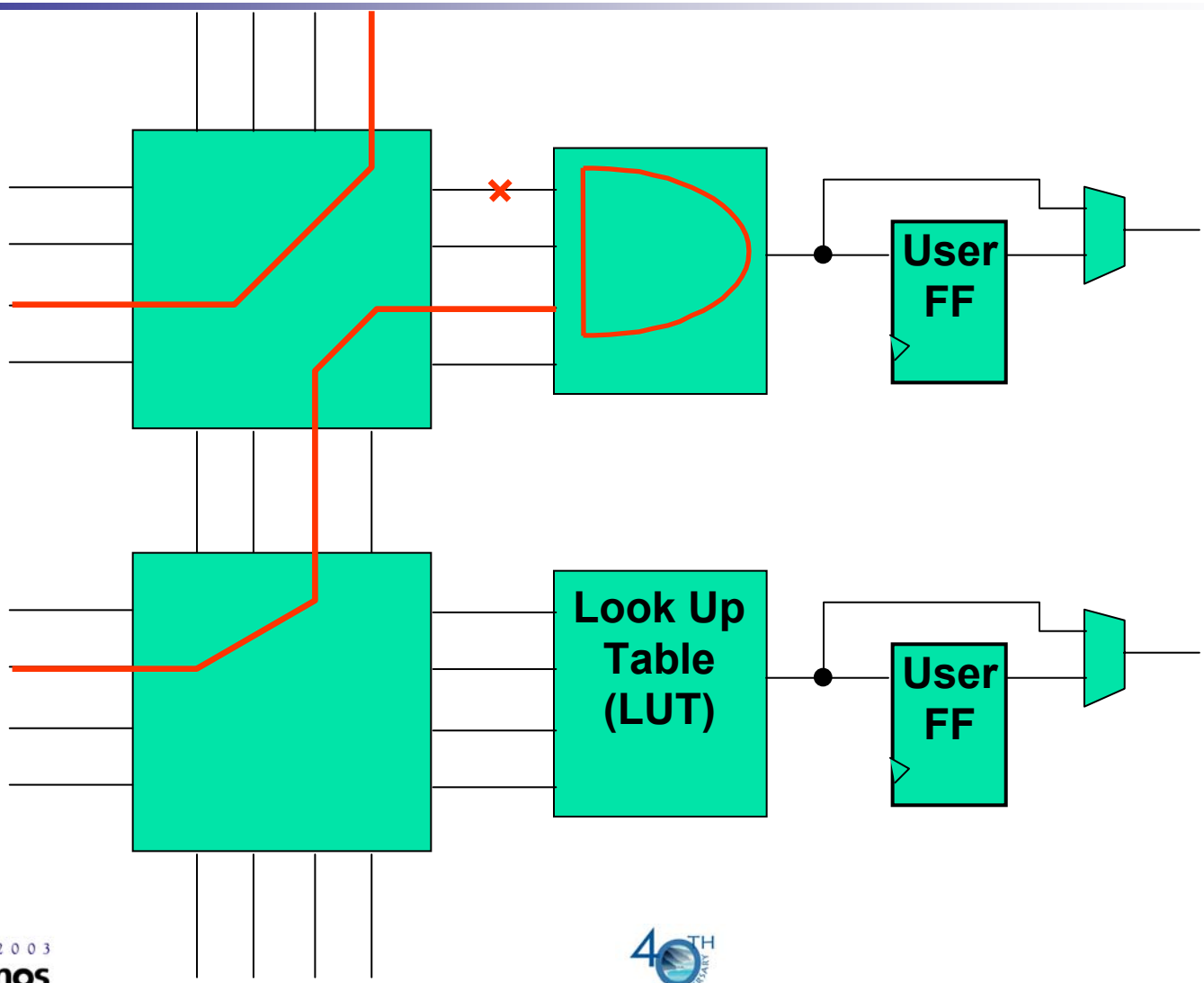
24,576 User Flip-Flops for XCV1000



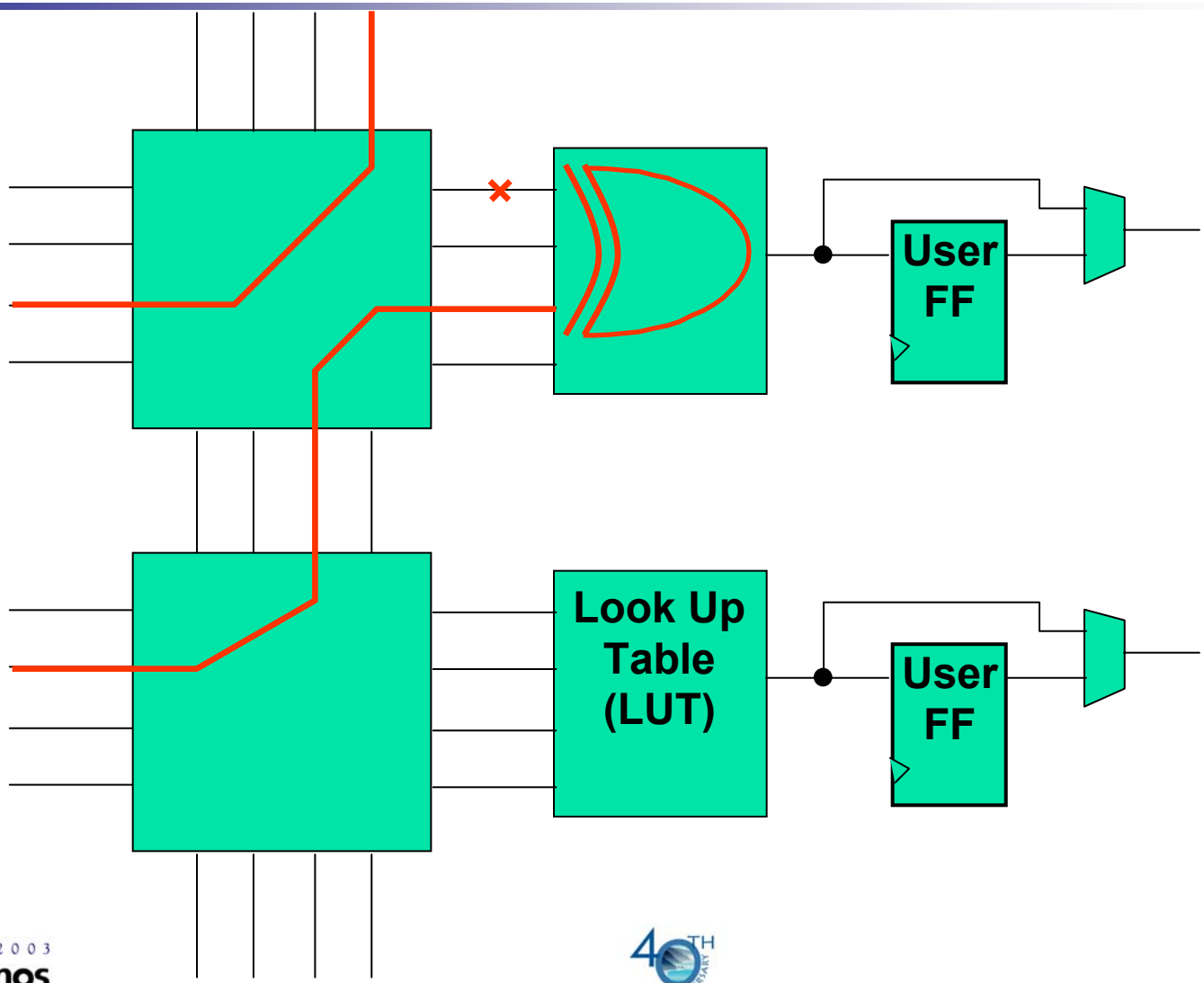
FPGA Design Implementation



FPGA Design - Routing Upset



FPGA Design - Logic Upset



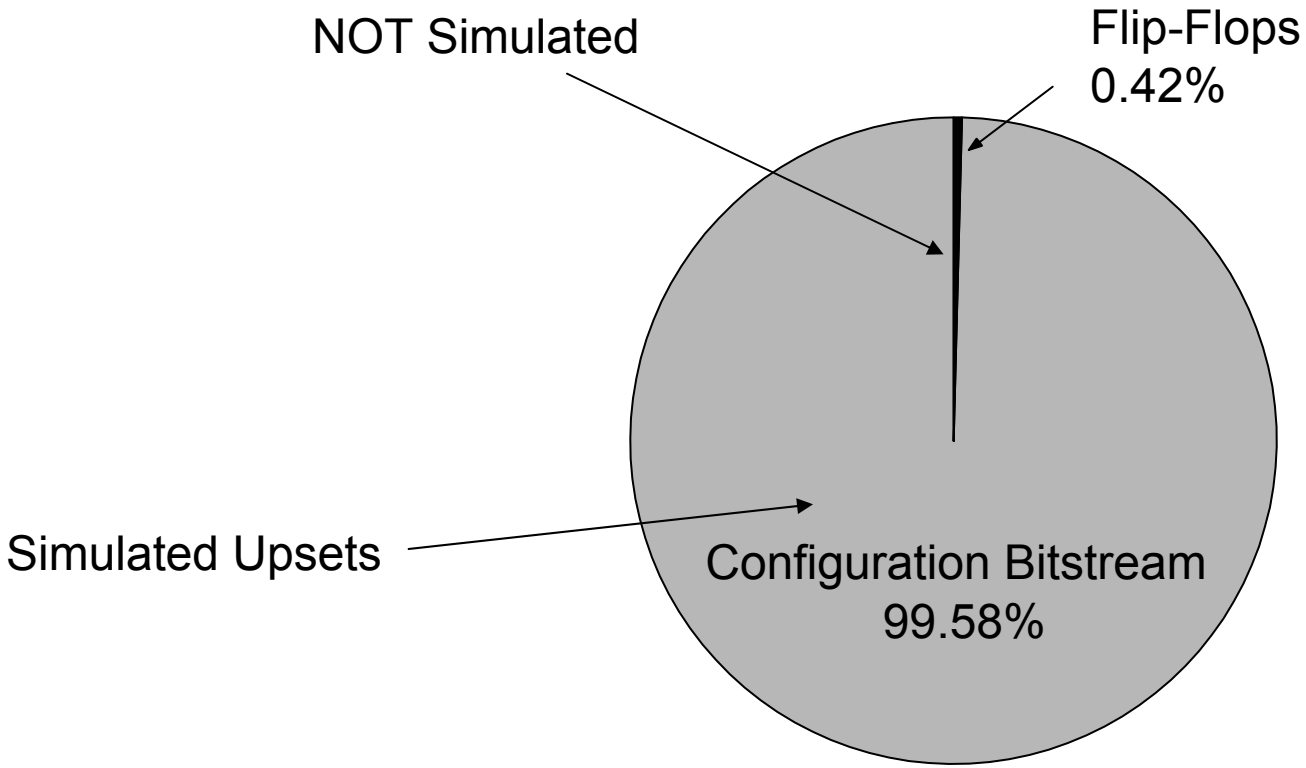
Configuration Bitstream Upsets

- Configuration upsets are *not* permanent and can be repaired at run-time
  - Upsets in configuration memory can be detected through the device *configuration readback*
  - Configuration faults can repaired through partial configuration
  - Readback and partial configuration can operate during circuit execution
    - With a few caveats (BRAM and LUT RAMs excluded)

Configuration Sensitivity

- Not all FPGA configuration bits affect dynamic design behavior
  - Many unused logic/routing resources for a design
  - Many "don't care" conditions within a design
- The "*Configuration Sensitivity*" of an FPGA design is the number of FPGA configuration bits that affect the design behavior.
  - Dependent on the design style and density
  - Only upsets of sensitive configuration bits will cause a design to fail

Total Static Cross-section of DUT*

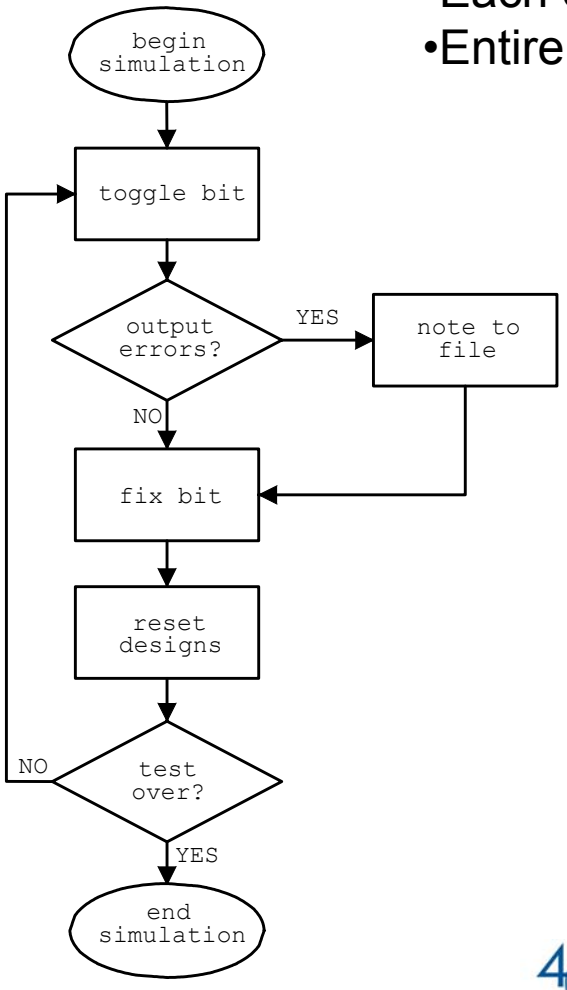


*Assumes Half-Latches are removed from Design[3][8]

SEU Simulator Concept [10]

- SEUs simulated by intentionally corrupting bits in the configuration bitstream while test design in operation
- Typically, only a single-bit upset is introduced at a time, though multi-bit upsets are possible.
- Output from a Design Under Test continually compared with "Golden" design.
- Configuration bits yielding output errors when upset are marked as "sensitive" and recorded in database *(database will be design dependent).*
- Many trials per bit provides a measure of the probability that a sensitive configuration bit will cause an output error
- Upset sequence not important

Simulation Procedure



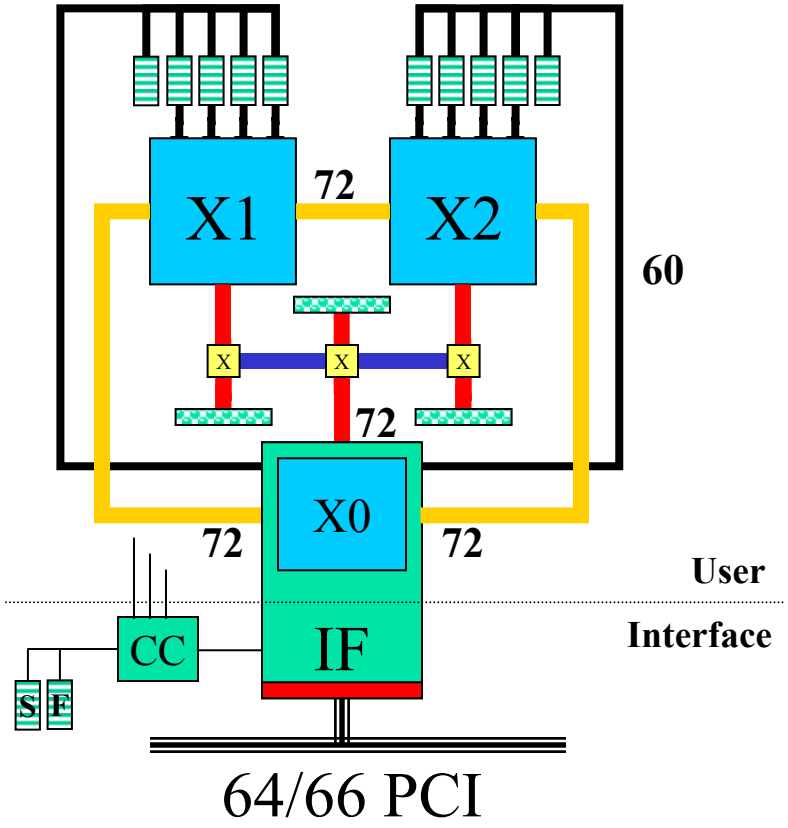
- Each cycle can be as little as 216 us
- Entire bitstream can be simulated in <25 min

Test Coverage

- Dynamic testing has problems with input vector test coverage
  - Both accelerator and simulator have these limitations
- We used LFSRs for Automatic Test Pattern Generation on the Mult/Add test designs
- On-orbit configuration SEUs persist briefly before repair, similar to simulation and accelerator testing

SLAAC-1V SEU Simulation Testbed

- Platform: SLAAC1-V
  - Developed at USC-ISI East as part of DARPA ACS program[6]
  - Supports high-speed partial reconfiguration and configuration readback
  - Open platform
  - Uses XCV1000 devices

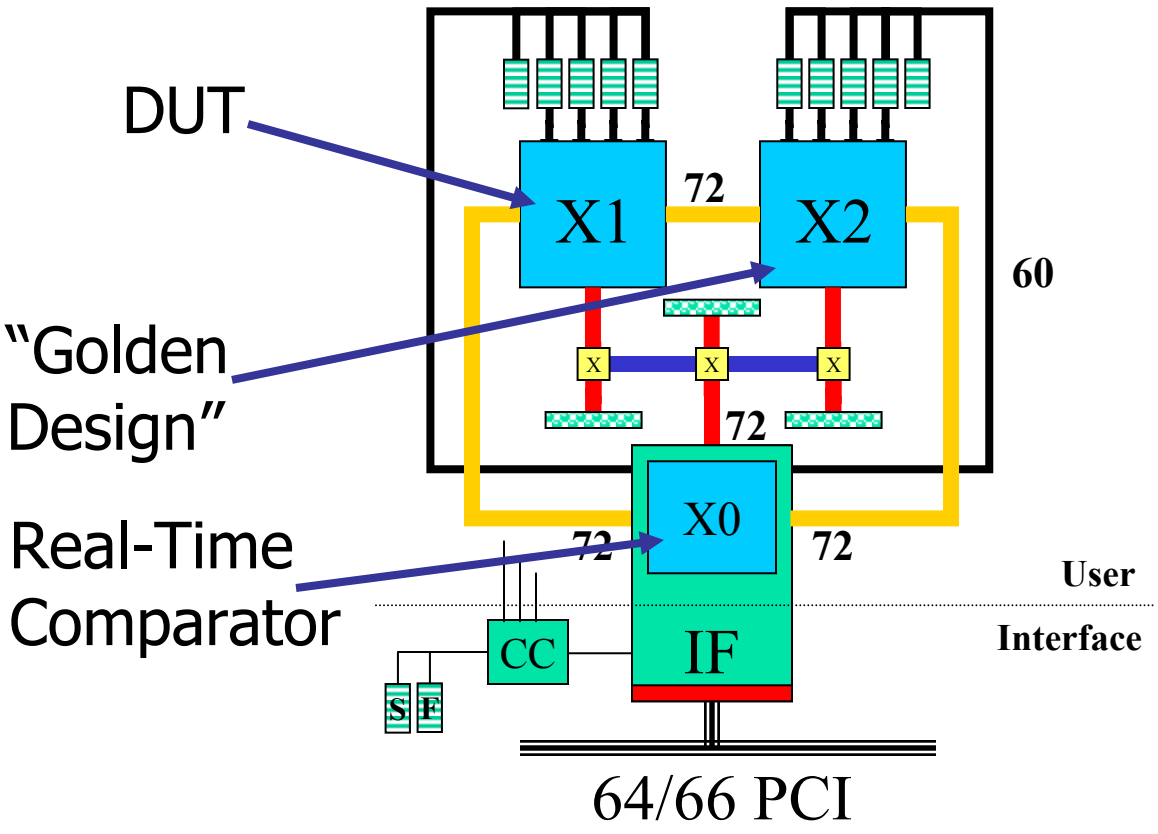


SLAAC-1V Proton Radiation Test Fixture

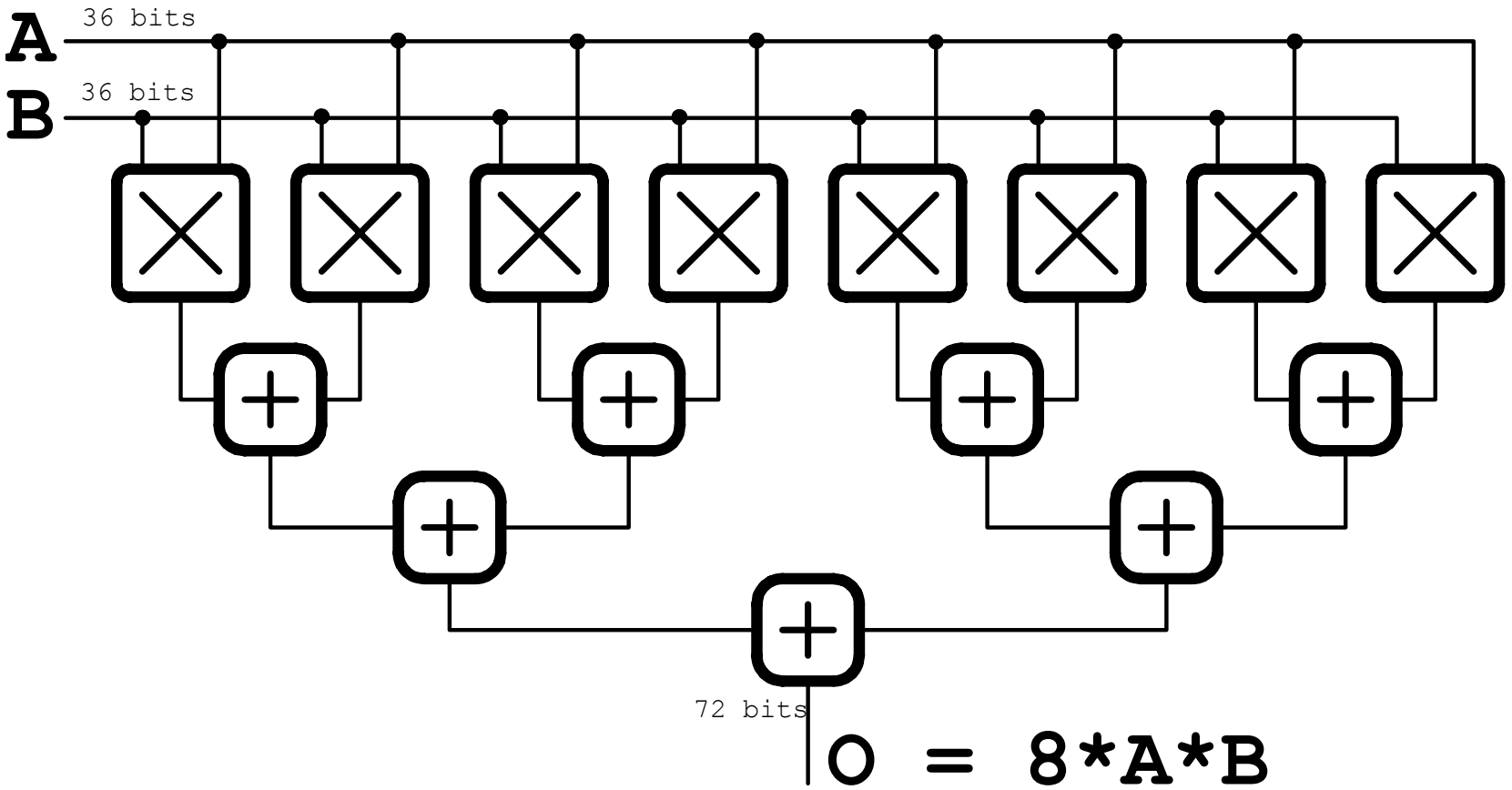
- Same platform used for SEU simulation except the *X1* FPGA was socketed.

- The DUT FPGA is irradiated while operating synchronously with the "golden design".

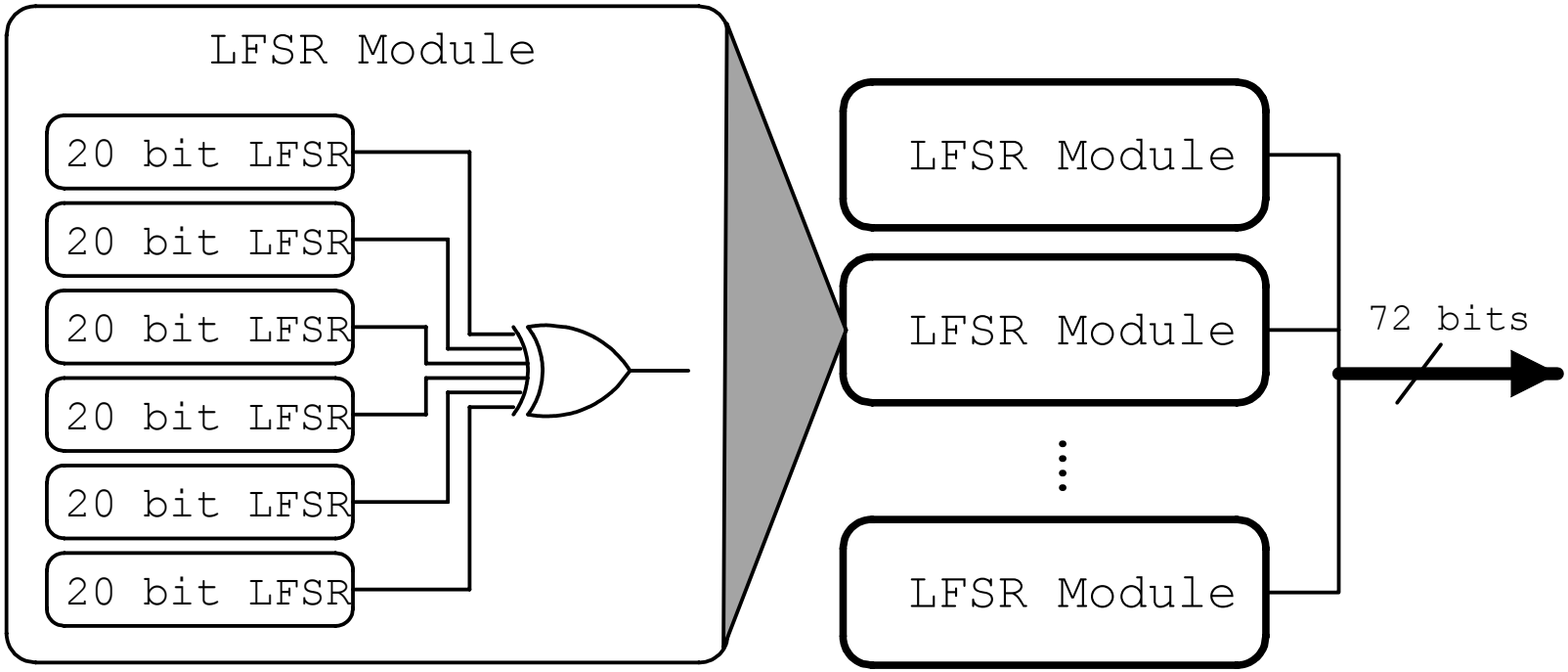
- *X0* provides design stimulus and compares outputs to identify errors



Multiply and Add Test Design



LFSR Test Design

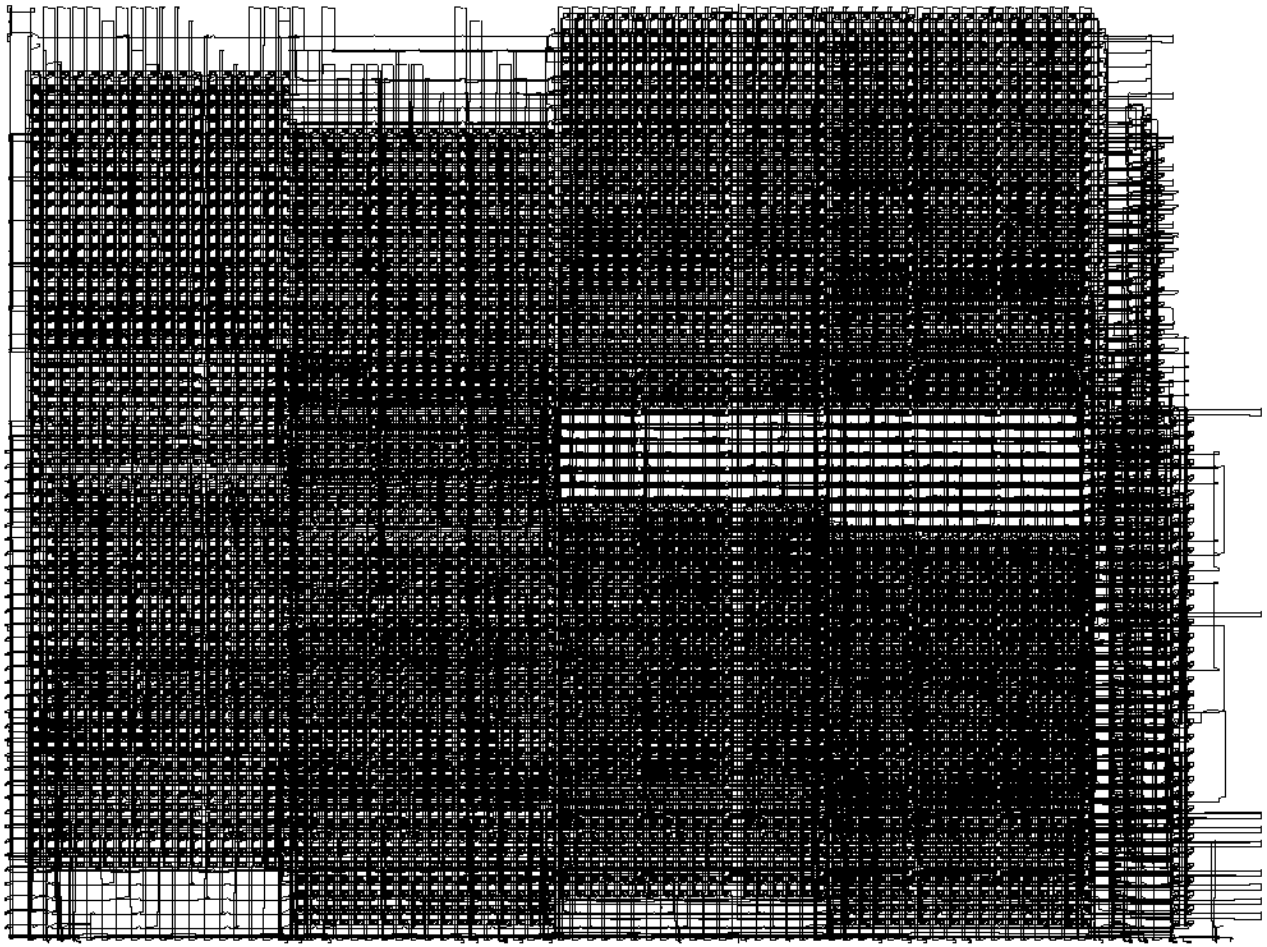


Test Design Utilization

Design	Slices	LUTs	Flip-Flops
72 Mult	8,308	10,872	15,264
36 Mult	2,206	2,844	3,744
72 LFSR	8,712	576	8,640

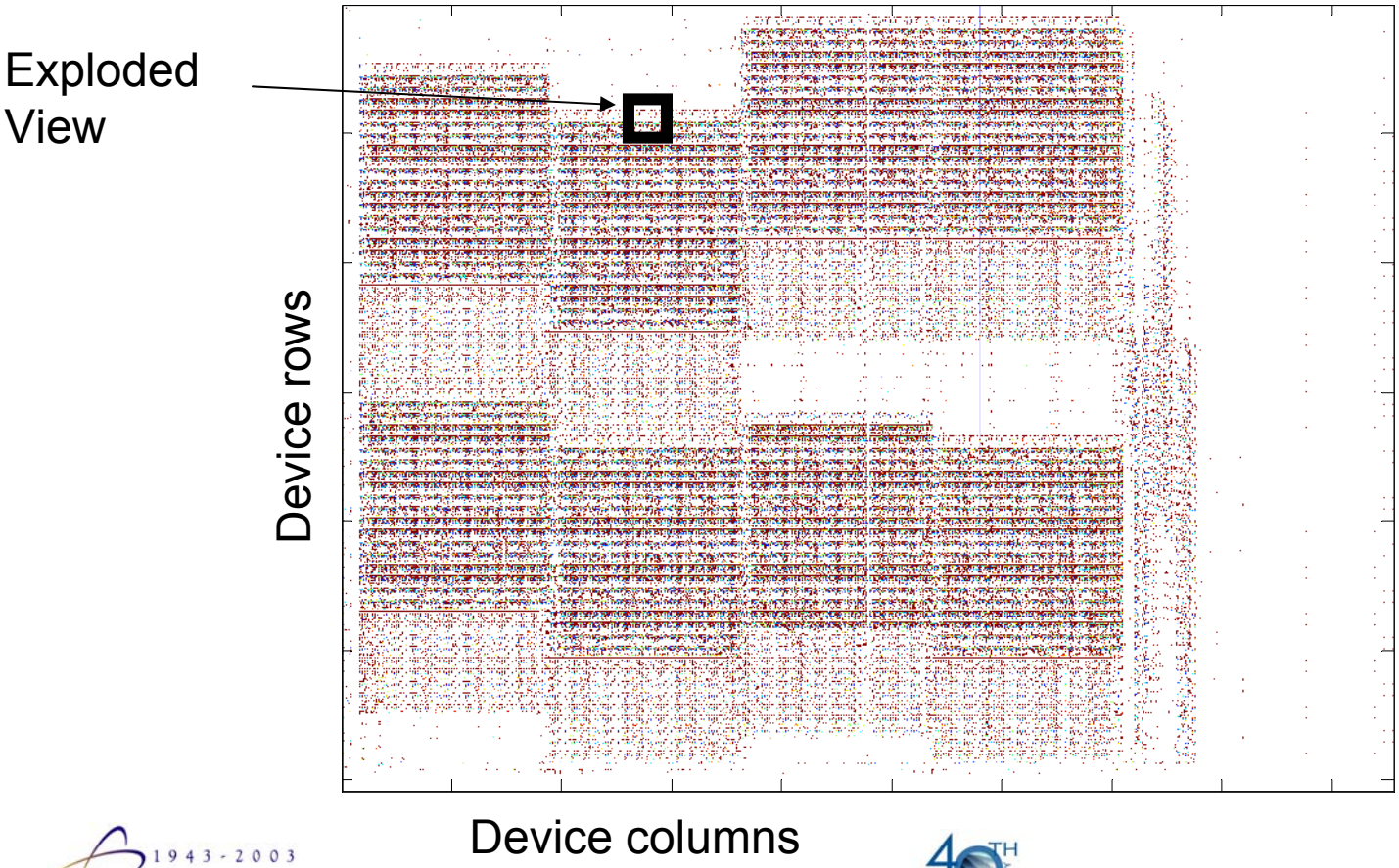
Designs simulated and tested in accelerator at 20 MHz (one trial at 2 MHz to test for clock dependency, none detected with available statistics).

Layout of 72-Mult Test Design

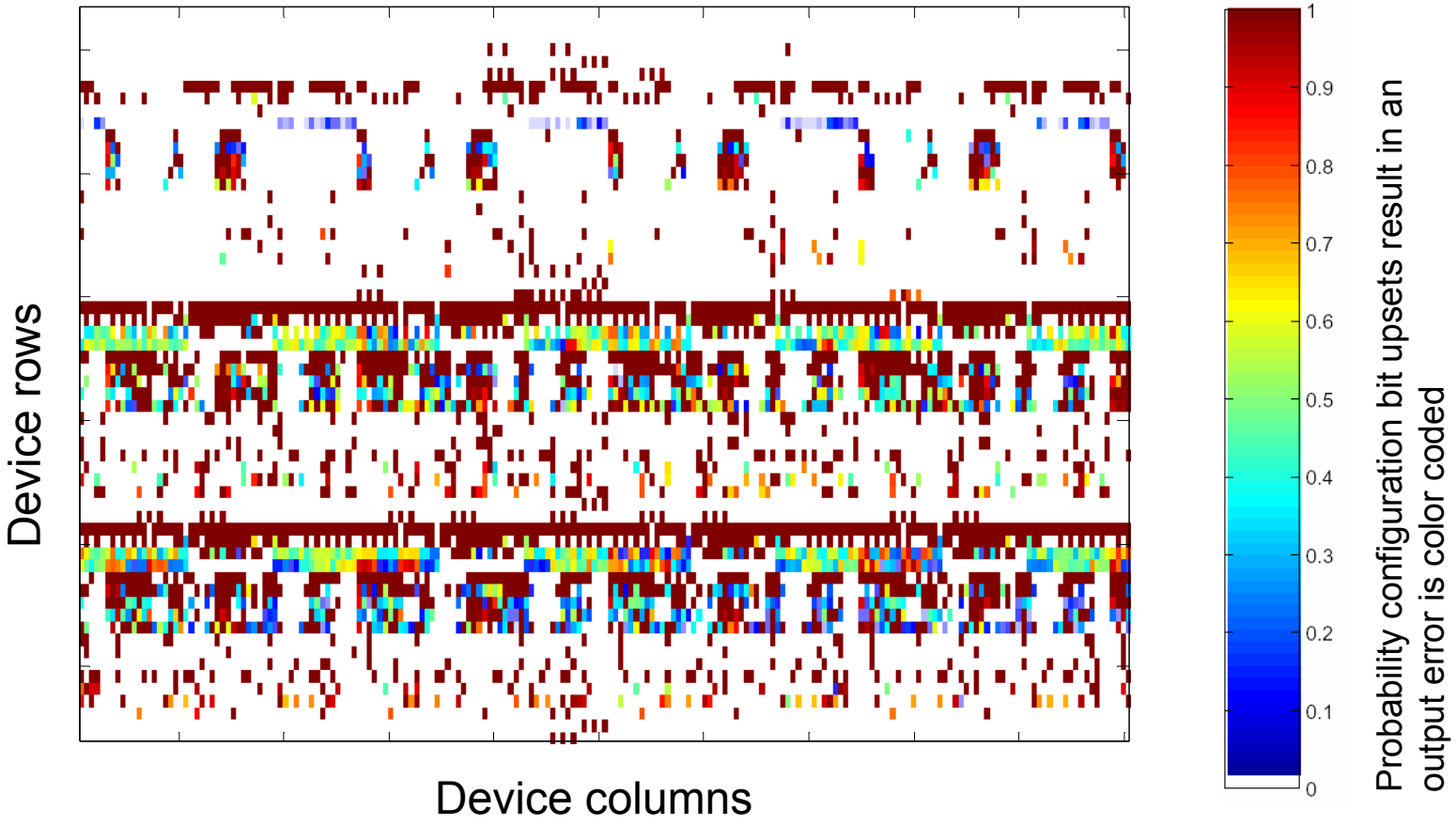


Simulation: Database Generated For 72-Mult Test Design

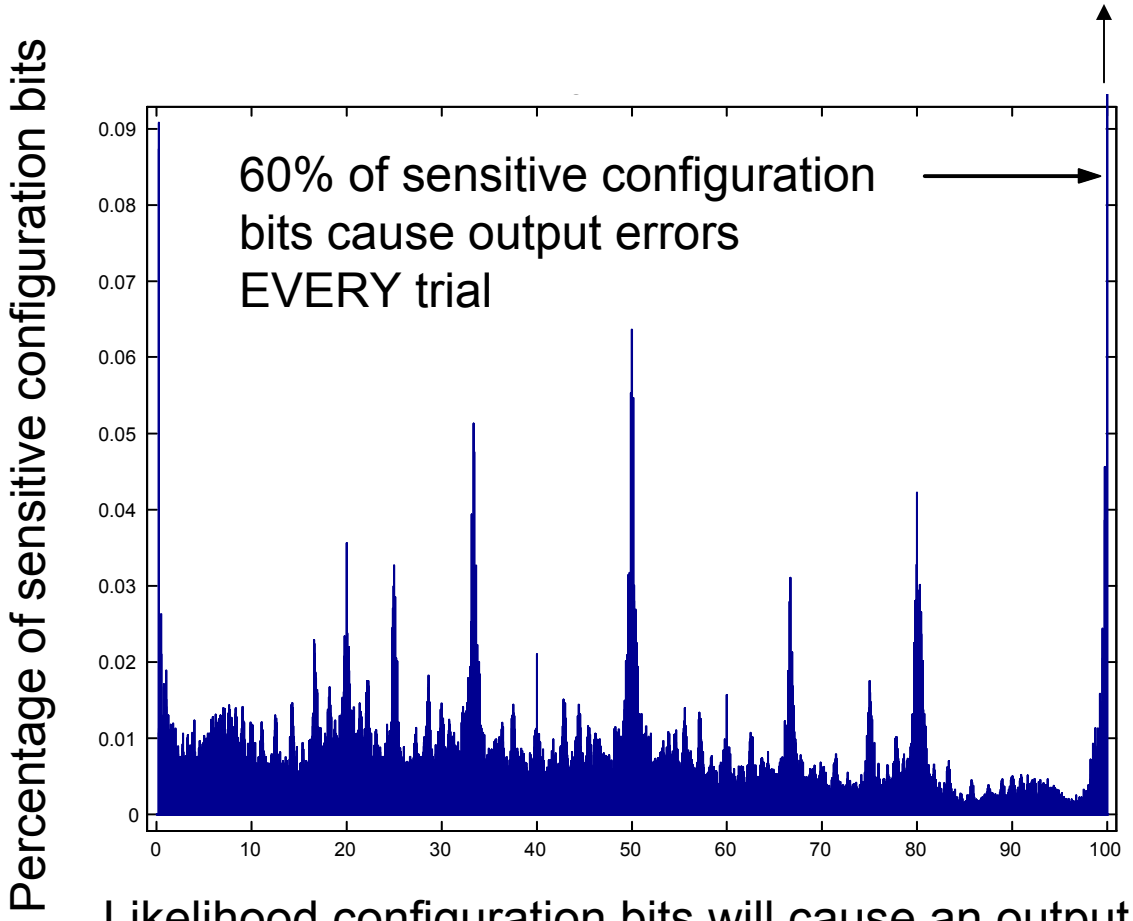
Contains probability of output error for each configuration bit, plotted geographically



Exploded View of Simulator Database



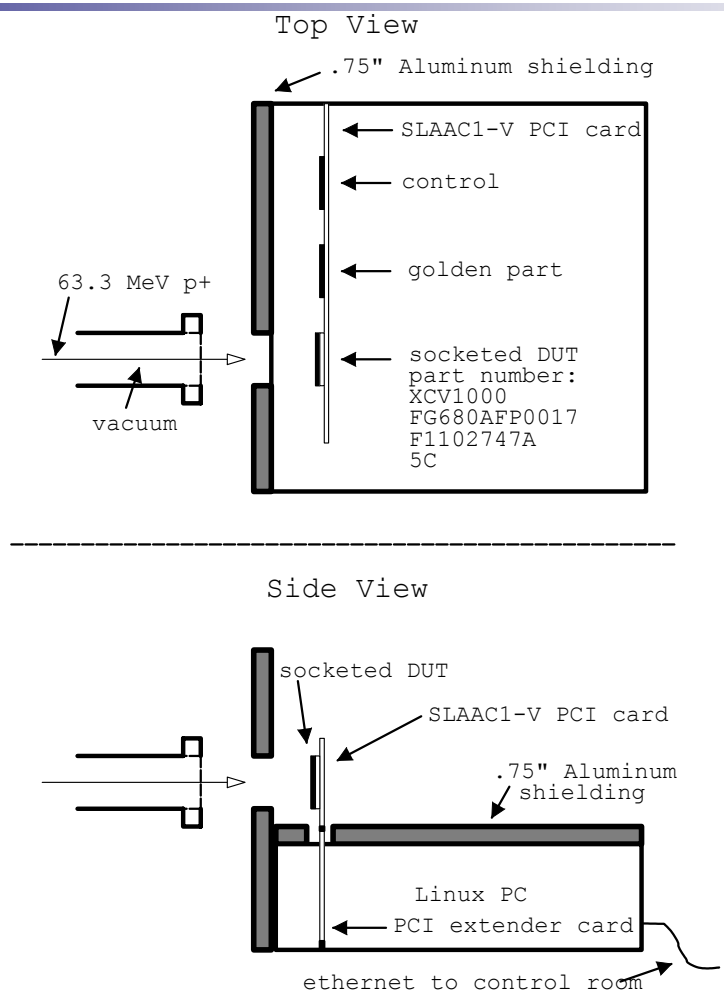
Simulator: Distribution of Database for 72-Mult



Accelerator Concept

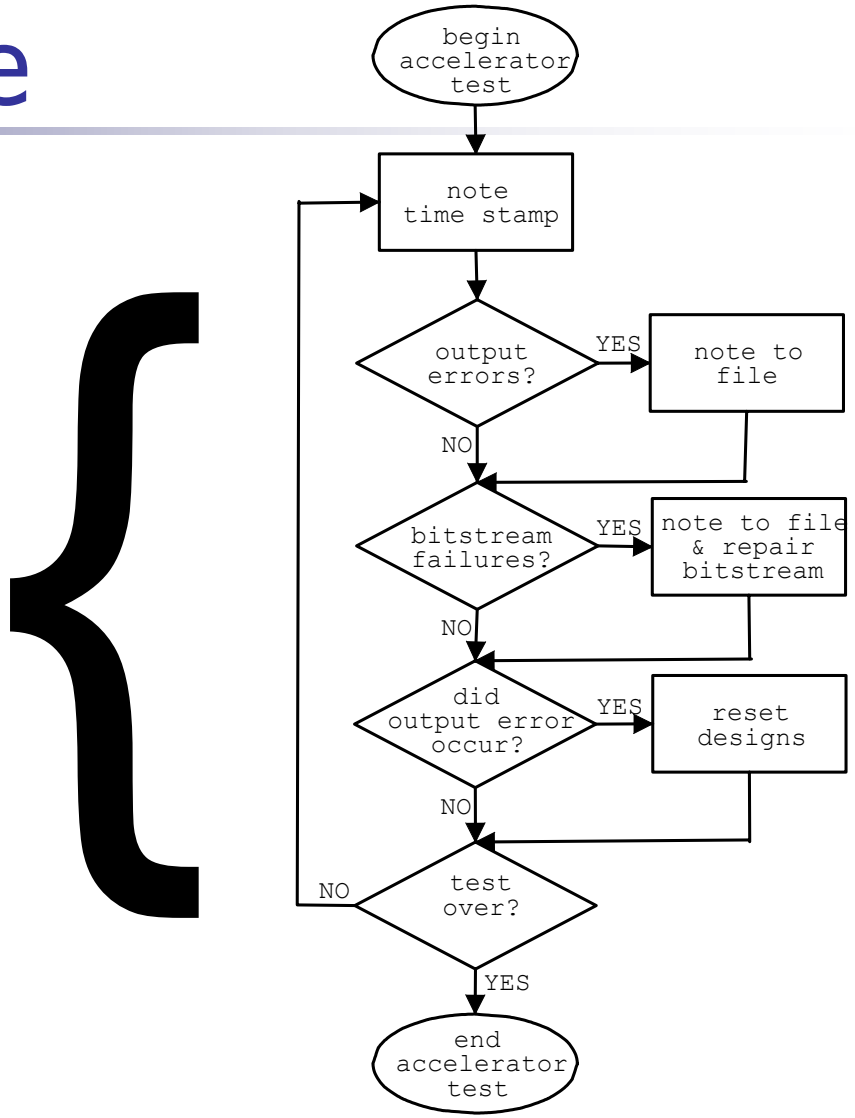
- SEUs slowly introduced with protons
- Monitor outputs for errors (Golden ≠ DUT) & note time
- Readback device configuration bitstream continually, note time and location of upsets
- Use partial configuration to repair bitstream upsets
- Reset DUT & Golden after output errors

Accelerator Test Setup

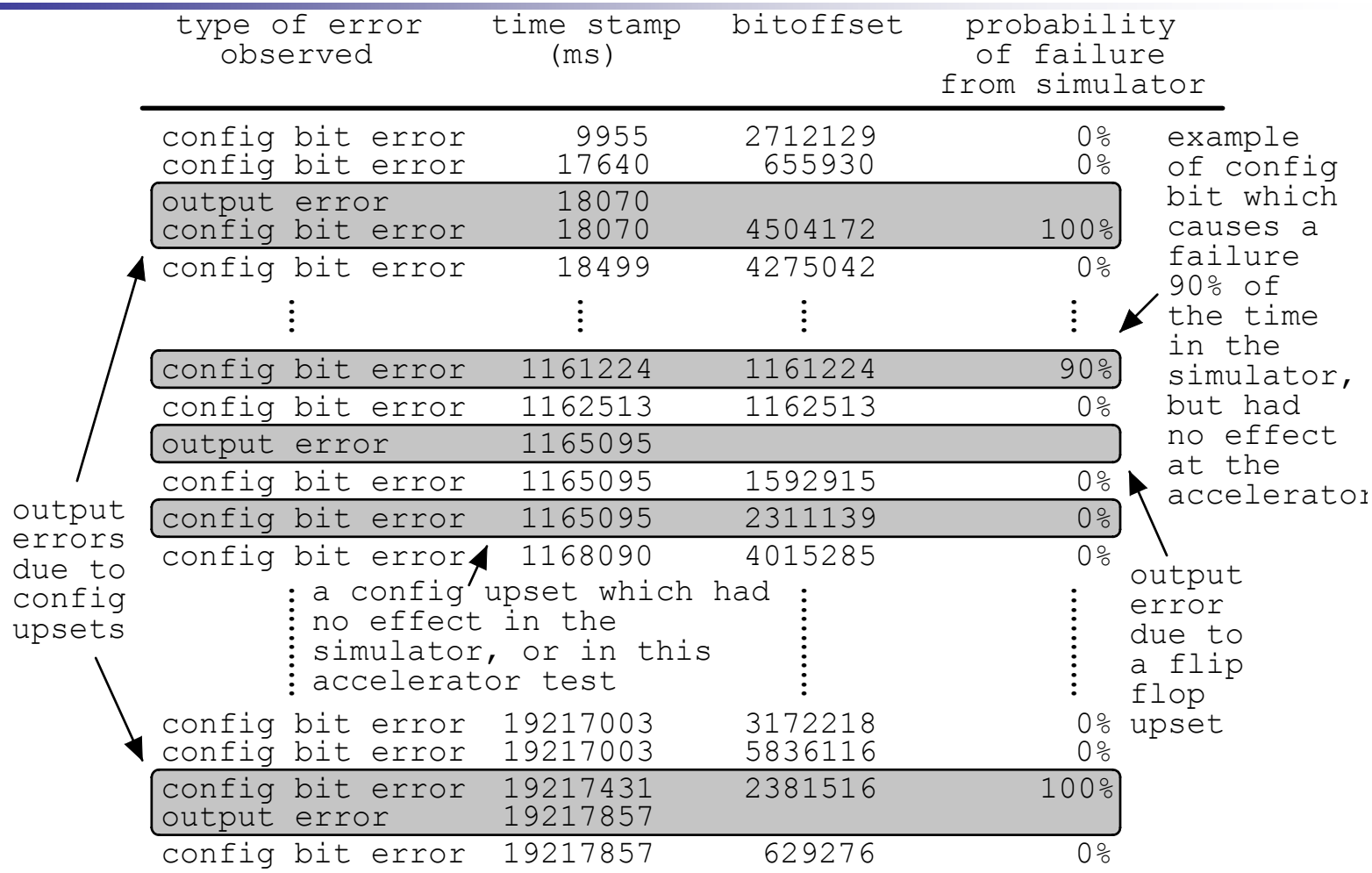


Accelerator Test Procedure

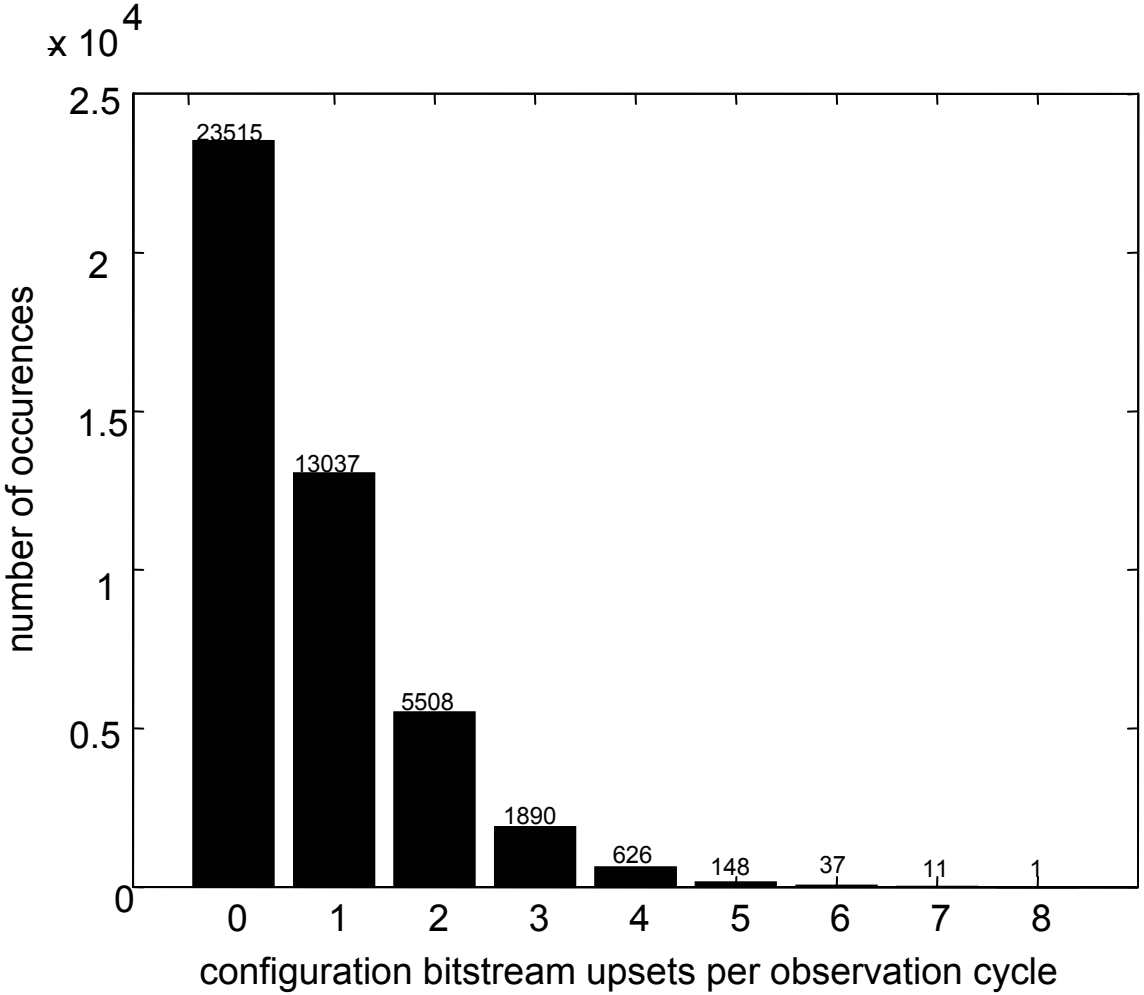
Observation Cycle
≈430ms



Accelerator: Example Results



Distribution of Configuration Upsets / Observation Cycle



Simulator vs. Accelerator: Average Fluence/Output Error

Design	Measured fluence to OE	Predicted fluence to OE
72-Mult	$7.8\times10^{7}\ \frac{p}{cm^2}$	$6.6\times10^{7}\ \frac{p}{cm^2}$
36-Mult	$2.6\times10^{8}\ \frac{p}{cm^2}$	$3.0\times10^{8}\ \frac{p}{cm^2}$
72-LFSR	$1.8\times10^{8}\ \frac{p}{cm^2}$	$2.0\times10^{8}\ \frac{p}{cm^2}$

OE - Output Error

Simulator vs. Accelerator

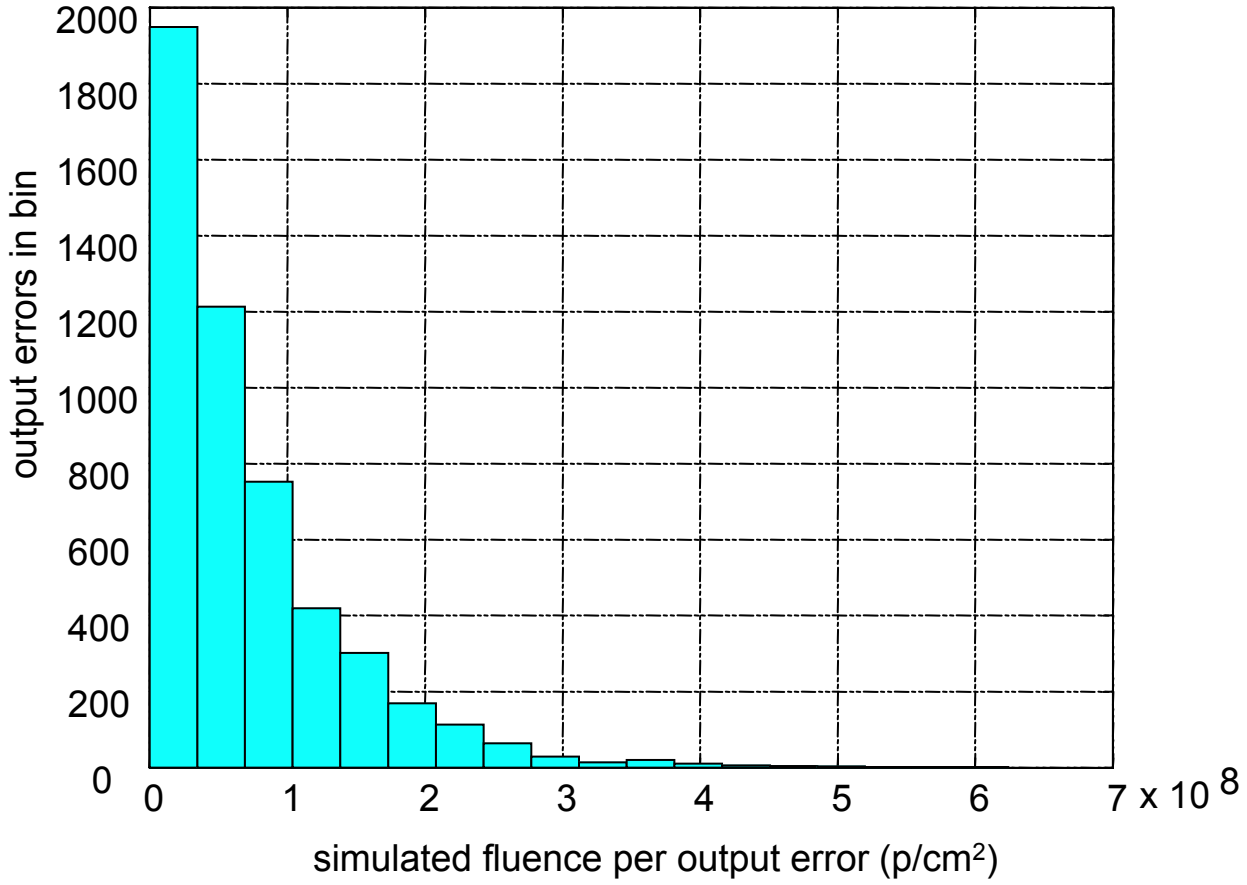
Percentage of observed output errors in accelerator predicted with simulator

Accelerator										Simulator		
Design	Duration (sec)	Fluence (p/cm^2)	CBUs	Fluence to CBU	POEs	Flip-Flop Errors	Fluence to OE	% POEs	% of sensitive CBs	OEs	CBUs	% of sensitive CBs
72-Mult	19267	3.9×10^{11}	33277	1.2×10^{7}	4958	108	7.8×10^{7}	97.8%	14.9%	3.6×10^{8}	2.32×10^{9}	15.4%
36-Mult	3694	3.8×10^{10}	3003	1.3×10^{7}	146	2	2.6×10^{8}	98.7%	4.9%	1.0×10^{8}	2.32×10^{9}	4.3%
72-LFSR	1019	1.1×10^{10}	1069	9.8×10^{6}	51	2	2.0×10^{8}	96.2%	4.8%	9.2×10^{7}	1.74×10^{9}	5.3%

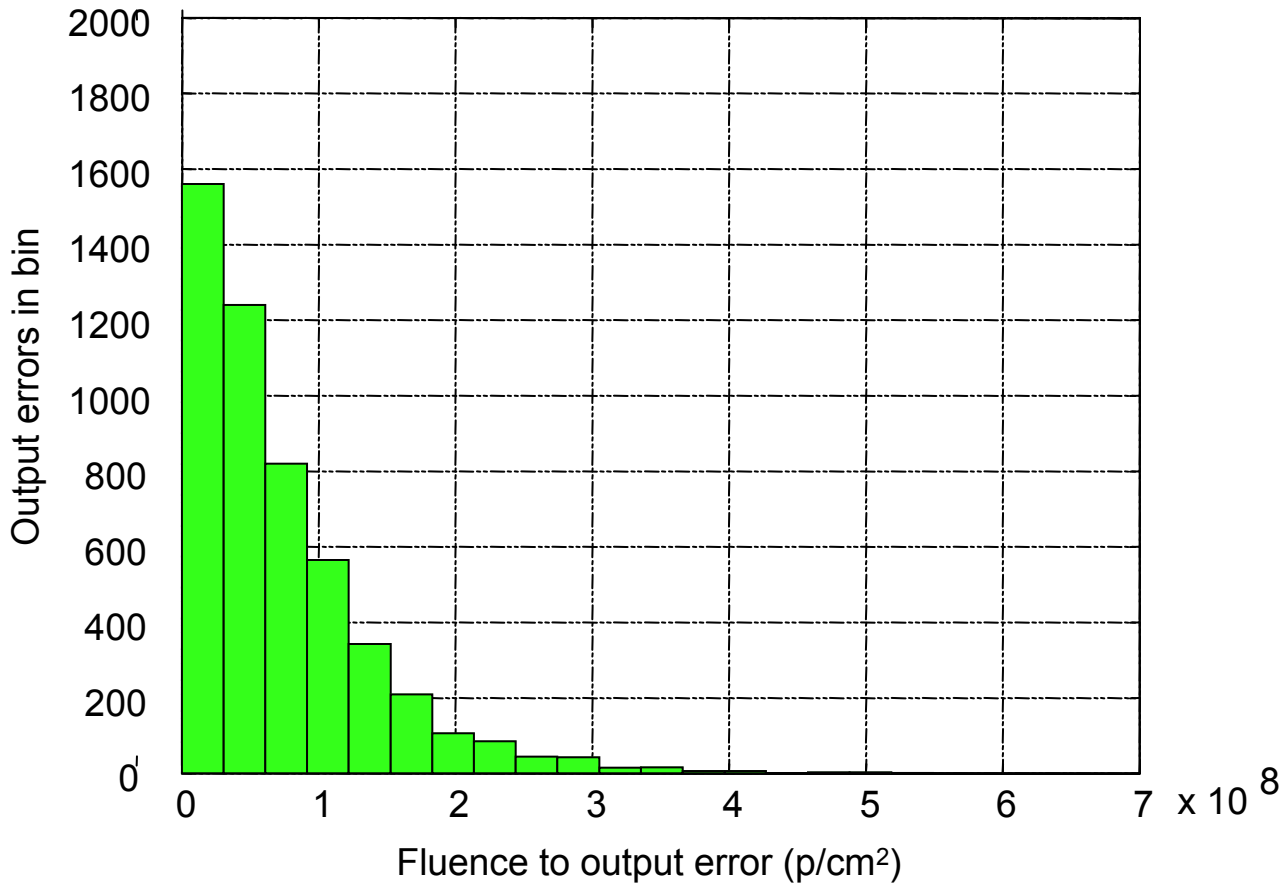
CBU - Configuration Bitstream Upset, POE - Predicted Output Error, OE - Output Error, CB - Configuration Bit

- Predicted output errors observed and Flip-Flop output errors
- Predicted vs. observed sensitive configuration bits

Simulator: Forecast Distribution of P^+ Fluence per Output Error



Accelerator: Measured Distribution of P^+ Fluence per Output Error



Conclusions

- Configuration bitstream dominates sensitive cross-section
- Simulator accurately tests configuration bitstream SEUs
  - Sensitive configuration bits identified
  - 98% Accurate in predicting output errors in comparison to accelerator
- Simulator accurately forecasts *DYNAMIC* design sensitivity
  - Dynamic sensitivity may be much lower than static cross-section may suggest => less frequent output errors
  - Not every configuration upset contributes to output errors
  - Sensitivity depends on design utilization & mitigation employed
- Simulator can now be used to:
  - Forecast dynamic behavior of a design in presence of configuration SEUs
  - Validate SEU mitigation strategies (design modifications for hardening)
  - Assure that mitigation strategies employed
    - Are not eliminated by design tools
    - Function as expected

References

1. Michael Caffrey. A space-based reconfigurable radio. In Toomas P. Plaks and Peter M. Athanas, editors, *Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA)*, pages 49–53. CSREA Press, June 2002.

2. E. Fuller, M. Caffrey, A. Salazar, C. Carmichael, and J. Fabula. Radiation testing update, seu mitigation, and availability analysis of the Virtex FPGA for space reconfigurable computing. In *MAPLD Proceedings*, September 2000.

3. Paul Graham, Michael Caffrey, Michael Wirthlin, Eric Johnson, and Nathan Rollins. Reconfigurable computing in space: From current technology to reconfigurable systems-on-a-chip. In *24th Annual IEEE Aerospace Conference*, 2003. To be published.

4. Eric Johnson, Michael J. Wirthlin, and Michael Caffrey. Single-event upset simulation on an FPGA. In Toomas P. Plaks and Peter M. Athanas, editors, *Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA)*, pages 68–73. CSREA Press, June 2002.

5. USC-ISI East. *SLAAC-1V User VHDL Guide*, October 1, 2000. Release 0.3.1.

6. Maria Geaorge and Peter Alfke. Linear feedback shift registers in virtex devices. Technical report, Xilinx Corporation, January 9, 2001. XAPP210 (v1.0).

7. Carl Carmichael, Michael Caffrey, and Anthony Salazar. Correcting single-event upsets through Virtex partial configuration. Technical report, Xilinx Corporation, June 1, 2000. XAPP216 (v1.0).

8. P. Graham, et al, "SEU Mitigation for Half-latches in Xilinx Virtex FPGAs," *IEEE Transactions on Nuclear Science*, December 2003, submitted.

9. C. Carmichael, "Triple module redundancy design techniques for Virtex FPGAs," Xilinx Corporation, Tech. Rep., November 1, 2001, XAPP197 (v1.0).

10. Michael Wirthlin, Eric Johnson, Nathan Rollins, Michael Caffrey, and Paul Graham. The reliability of fpga circuit designs in the presence of radiation induced configuration upsets. In *Proceedings of the IEEE Symposium on FPGAs for Custom Computing Machines (FCCM '03)*. IEEE Computer Society, 2003. To be published.

Acknowledgements

- The authors would like to thank Xilinx and, specifically, Carl Carmichael and Joe Fabula for their support of this work.
- We would also like to thank the University of Southern California's Information Sciences Institute (USC/ISI) for their support of our SEU simulation work.
- We acknowledge the Department of Energy's funding of this work through the Deployable Adaptive Processing Systems project and Cibola Flight Experiment.